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San Jose State UNIVERSITY ColleGe of engineering

Introduction to NMOS Digital Logic

College of Engineering San Jose State University

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Chapter 1: Introduction **to NMOS FETs**

To complete this project, you will simulate, build, test, and document a circuit that demonstrates basic functions of an NMOS FET, and the voltage across the gate and source controls the drain source current as shown by equation x, and they are three models of the transistor based on the equation. The first model is an open circuit when the VGS is less than the threshold voltage, the second model is linear VGS is more than the threshold voltage and the difference of VGS and the threshold voltage more than the VDS, and the third model is in saturation and is when VGS is more than the threshold voltage and the difference of VGS and the threshold voltage less than the VDS.

(Equation 1)

The simulations will be run from the files from [this folder](https://github.com/ElisaParent/Intro-to-NMOS-Digital-Logic/blob/main/20250724%20Traditional%20NMOS%20Techology.zip), and three simulations will be used to show the characteristics of an NMOS.

A diagram of a circuit

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Fig. 1 NMOS circuit with stepping the drain voltage, and varying the gate voltage as the independent variable

A graph of different colored lines

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Fig. 3 Simulation of varying VGS and plotting IDS with Vds at 1.25V and the schematic used to create this graph is in file 20250717 NMOS FET testing with steady VDS

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Fig. 4 Simulation of varying VGS and plotting IDS six times, and each time stepping up the VDS by one V, starting at zero, and the schematic used to create this graph is in file 20250717 NMOS FET testing varying VGS

Chapter 2: Introduction **to NMOS Logic Gates**

# Introduction

This lab will show you how to create input vs output simulations of NMOS logic gates and show the improvements with each circuit design.

# Objective

After successfully completing the work outlined in this lab, students should be able to use LTspice to generate common signals to test NMOS logic gates.

# Theory:

Logic gates (NOR, NAND and NOT gates) create some of the basic building blocks for digital logic and are needed to compute operations in Boolean algebra, and the simplest model is to use is truth tables. The issue is making sure the logic gates are performing as close to ideal as possible.

Table 1: Truth Table for NOT Gate

|  |  |
| --- | --- |
| Input | Output |
| 0 | 1 |
| 1 | 0 |

Table 2: Truth Table for NOR Gate

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Table 2: Truth Table for NAND Gate

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# LTspice simulations for NMOS Logic Gates:

The first set of simulations for the NMOS Logic Gates is the NOT Gate or Inverters, To test the NOT gates, run both the file with the dc sweep (20250717 Inverter Testing DC) and transient response (20250717 Inverter Testing transient) to test the NOT gates plus the derivative of the output because when it crosses one or negative one, it can signal a change in logic level.

A diagram of a computer

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Fig. 5 NOT gate testing schematic, with the leftmost with the load as a resistor, the middle with a NMOS FET diode connected load, and the rightmost with a NMOS FET with the load gate higher than the load drain as to make sure it is in saturation

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Fig. 6 Input vs output of NOT gate by doing a DC sweep of the input

A graph with colored lines

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Fig. 7 Change of output over input using doing a DC sweep of the input

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Fig. 8 Output over time of NOT gate varying input using a square wave

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Fig. 9 Gain voltage vs time for NOT gate varying input using a square wave

The second set of simulations for the NMOS Logic Gates is the NOR gates, and to test the NOR gates, run transient command to test the NOR gates plus the derivative of the output because when it crosses one or negative one and goes back to zero, it can signal a change in logic level. The file name is 20250717 NOR gate testing.

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Fig. 10 NOR gate testing schematic, with the leftmost with the load as a resistor and the rightmost with a NMOS FET diode connected load

A white screen with different colored lines

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Fig. 11 Input, Output, and Gain of NOR gate varying input using a square wave

The second set of simulations for the NMOS Logic Gates is the NAND gates, and to test the NAND gates, run transient command to test the NAND gates plus the derivative of the output because when it crosses one or negative one and goes back to zero, it can signal a change in logic level. The file name is 20250717 NAND gate testing.

A diagram of a machine

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Fig. 12 NAND gate testing schematic, with the leftmost with the load as a resistor and the rightmost with a NMOS FET diode connected load

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Chapter 3: Introduction to Traditional NMOS SRAM

# Project: NMOS SRAM

# Introduction

This lab will show you how to test a traditional NMOS SRAM with a clock cycle and having write and reset alternating being off and on

# Objective

After successfully completing the work outlined in this lab, students should be able to use LTspice to generate basic input and output curves using LTspice for an SRAM, using the file 20250717 SRAM testing and the testing setup used by Dr. Faquir Jain.

A diagram of a circuit

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Fig. 14 Schematic of NMOS SRAM

A diagram of a graph

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Fig. 15 Input, Output, and Gain of NMOS SRAM varying input using a square wave